In the Claims:

1-34. (canceled)

35. (currently amended) A system comprising:

A. a memory containing instructions;

B. a main processor unit coupled to the memory and executing instructions obtained from the memory;

C. a stack machine, separate from the main processor unit, coupled to the memory and executing instruction bytecodes obtained from the memory, the stack machine including:

i. a program counter containing an address of a first instruction bytecode to be decoded;

ii. a program counter calculator coupled to the program counter and providing the program counter with the address of the first instruction bytecode to be decoded, the program counter calculator including a match input;

iii. a register containing instruction bytecodes including the first instruction bytecode and a second instruction bytecode following the first instruction;

iv. decode logic coupled to the register and to the program counter calculator and decoding the first instruction bytecode from the register; ~~and~~

v. pre-decode logic having a match output connected with the match input of the program counter calculator and being coupled to the second instruction bytecode in the register, the pre-decode logic decoding the second instruction bytecode while the decode logic is decoding the first

instruction bytecode and selectively providing a match signal to the program counter calculator to increment the program counter past the second instruction bytecode; and

vi. the register having instruction sections, each section containing an instruction bytecode, the pre-decode logic includes sets of comparator logic, each comparator logic set has inputs coupled with one instruction section and an output, and the pre-decode logic includes multiplexer circuitry having inputs connected to the outputs of the comparator logic sets and a match output connected with the program counter calculator.

36. (canceled)

37. (previously presented) The system of claim 35 in which the register has instruction sections, each section containing an instruction bytecode, and the number of sections is greater than the number of instruction bytecodes in the longest instruction.

38. (previously presented) The system of claim 35 in which the pre-decode logic decodes a prefix in the second instruction bytecode.

39. (currently amended) A process of operating a system comprising:

A. placing instructions in a memory;

B. executing instructions obtained from the memory in a main processor unit coupled to the memory;

C. executing instruction bytecodes obtained from the memory in a stack machine coupled to the memory;

D. incrementing a program counter in the stack machine to contain an address of a first instruction bytecode to be decoded;

E.. providing the program counter with the address of the first instruction bytecode to be decoded from a program counter calculator having a match input;

F. moving instruction bytecodes including the first instruction bytecode and a second instruction bytecode following the first instruction bytecode into a register;

G. decoding the first instruction bytecode in the register in decode logic coupled to the register and to the program counter calculator; ~~and~~

H. while decoding the first instruction bytecode, pre-decoding at least the second instruction bytecode in pre-decode logic coupled to the register, and selectively providing a match signal from a match output of the pre-decode logic to the match input of the program counter calculator to increment the program counter past the second instruction bytecode;

I. the moving including moving instruction bytecodes into register sections, each section containing an instruction bytecode, and the pre-decoding includes comparing the instruction bytecode in each instruction section with a known prefix and producing a section output, and multiplexing the section outputs to the match output.

40. (canceled)

41. (previously presented) The process of claim 39 in which the moving includes moving instruction bytecodes into register sections, each section containing an instruction byte, and the number of sections is greater than the number of instruction bytecodes in the longest instruction.

42. (previously presented) The process of claim 39 in which pre-decoding logic pre-decoding a prefix in the second instruction bytecode.